UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,611	02/04/2004	Tyler J. Gomm	303.816US2	3437

21186 7590 10/19/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
1600 TCF TOWER
121 SOUTH EIGHT STREET
MINNEAPOLIS, MN 55402

EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,611	GOMM ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,8,10-14,16-18,26 and 30* is/are allowed.

6)☒ Claim(s) *1,3,5-7,9,15,19-25,27-29 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

Reference No. 6,476,594 has not been considered because the listed reference does not correspond with the name of the applicant cited, the publication date, and the filing date cited. It is not clear to the examiner which patent applicant wants to be considered. All other references have been considered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-7, 15, 19-25, 27-29, and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (U.S. Patent No. 6,421,789) in view of Matsuzaki (U.S. Patent No. 6,088,255).

In reference to claim 1, Ooishi discloses in Figure 1 a memory device comprising: an input node (P1) for receiving an external signal (CLK); a memory array (MA) having row and column of memory cells; a row decoder (10) connected to the memory device; a column decoder (14) connected to the memory device; an output data path (P13, 22, G-I/O) for transferring of data between the cells and data lines (see column 7, line 63 through column 8, line 5); and a circuit (30) for generating an internal signal. Ooishi does not disclose that the circuit (30) includes a plurality of measuring delay elements; an interval controller; and a plurality of correction delay elements. Matsuzaki discloses

in Figure 15 a plurality of measuring delay elements (1050; see also Figure 19) connected to the input node for delaying the external signal (CLK1) during a measurement to produce a measured delay, wherein the measurement is set to last for at least one cycle time of the external signal (see column 23, lines 39-54); an interval controller (1060) connected between the input node and the measuring delay elements (1050) for controlling the frequency of the measurement (see column 23, line 39-54); and a plurality of correction delay elements (1021) connected to the input node for delaying the external signal (CLK1) based on the measured delay to generate an internal signal. Since Ooishi does not disclose the particulars of the circuit (DLL 30), it would have been obvious to one skilled in the art at the time of the invention that any DLL circuit capable of generating an internal signal based on an external signal could be used to control the transfer of the data in the circuit of Ooishi and the circuit (Figure 15) of Matsuzaki discloses an example of such a circuit providing the benefit of setting the corrected delay in a short time. The same applies to claims 5, 15, 19, 24, 28, and 31 wherein the decoding circuit is equivalent to the row and column decoder and while the processor is not shown, it is considered to be well known to one skilled in the art the memory devices such as the one disclosed by Ooishi may be connected to processors.

In reference to claim 6, Matsuzaki discloses in Figure 19 that the measuring unit includes a delay model (1025) connected to an output node of the interval controller (1060) for delaying a signal outputted at the output node of the interval controller (1060). The same applies to claims 20, 21, and 34 (wherein the number represents the number of delay elements the start signal passes through).

In reference to claim 7, Matsuzaki discloses in Figure 19 that the measuring unit (1050) includes a converter (1050-N, 1005-N) connected between the output node of the delay model (1025) and the adjusting unit (1021) for converting the reference time into a measured delay. The same applies to claim 25.

In reference to claim 9, Matsuzaki discloses in Figure 22, 24 that the adjusting unit (1021) includes a plurality of correction delay elements connected between the input nodes of the memory device and the output nodes of the adjusting unit (1021). The same applies to claims 22, 27, and 35.

In reference to claim 23, Matsuzaki discloses in Figure 20 that the time interval between consecutive measurements among the number of measurements is greater than the cycle time of the external signal (CLK1). The same applies to claims 29 and 32.

In reference to claim 33, Matsuzaki discloses in Figure 20 that the external signal (CLK1) has a frequency equal to a multiple of a frequency of the start signal (START).

In reference to claim 36, Matsuzaki discloses in Figures 19 and 24-25 that the number of measuring delay elements and a number of correction delay elements are equal.

Allowable Subject Matter

3. Claims 2-4, 8, 10-14, 16-18, 26 and 30 are allowed.

4. The following is an examiner's statement of reasons for allowance: Claims 2-4, 8, and 16-18 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 7 which includes a frequency modifier (710) for setting the time

interval between one measurement and the next measurement to be unequal to a cycle time of the external signal (XCLK) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 10-14 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 7 which includes a frequency divider (710) located on the first path for dividing a frequency of the external signal (CLKIN) to control a frequency of the measurement such that the frequency of the measurement is unequal to the frequency of the external signal (CLKIN) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 26 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 1 wherein producing the reference time (T_{REF}) includes subtracting the model delay time (T_{DL}) from at least one cycle time of the external signal (MT_{CK}) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 30 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the stop signal (STOP) is shifted from the start signal (START) by at least one cycle of the external signal (XCLK) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
October 16, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800